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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,604	03/20/2001	Larry Leighton	257/265	3015

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/813,604	LEIGHTON ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 March 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show in Fig. 1(b) item 5 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because the bracket on line 6 is not closed while a comma just prior to it should be removed. Correction is required. See MPEP § 608.01(b).

4. Furthermore, the interconnection between the lower extremities of wires 23 and 25 to the right of item 6 on Fig. 1(b) is not stipulated expressly in the disclosure.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 1 – 4 and 9 - 12 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Kagawa (5,371,405) in view of Nishiuma et al (JP404048756A).

With regard to claim 9, and with reference to Fig. 1(a): Kagawa teaches a high-power transistor (cf. title) comprising

a substrate 2 (cf. Fig. 1(a) and column 2, line 38);

a transistor chip or die 5 secured to the substrate (cf. column 2, line 67-68), the die comprising a transistor (die is called 'transistor chip') having an input terminal (cf. claims 1 and 12 in Kagawa) (the terminal connected to wire 22 (cf. column 3, line 15));

an input matching element in the form of a MOS capacitor 7 (cf. column 3, lines 29-34) (or any other capacitor; see column 2, lines 59-62) secured to the substrate by means of ground pad 3 (cf. column 2, line 41); and

one or more wires (wire 22) coupling the transistor die 5 (or 6: 5 and 6 point to the same component type in all figures) electrically coupling the transistor input terminal to the input matching element 7.

Kagawa does not necessarily teach the impedance of wire 22 to be based in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

However, it is widely known in the art of high-frequency power transistors that particularly for high-frequency applications the impedance of the wires is important and needs to be tailored to other device components, as witnessed by Nishiuma et al, who teach to make the impedance of a bonding wire to coincide with the impedance of a signal line as part of the design of a semiconductor integrated circuit for high-frequency signal propagation (see 'abstract', first sentence, and 'constitution', final sentence). Furthermore, the bonding wires, being the final components to be added to the device as a whole, are the last components of which the impedance is still controllable, after the transistor die has been secured to the substrate. It thus would be obvious to measure the impedance characteristics of the die thus secured to the substrate prior to selecting the impedance of the wire for the purpose of impedance control of the IC. In summary, it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the stipulation in claim 9 that the impedance of the said one or more wires be selected or based at least in part on the performance characteristics of the transistor as measured after the die is secured to the substrate.

With regard to claim 10: because matching of one impedance to another impedance is an important parameter to control, as witnessed for instance by the

matching of the impedance of said bonding wire to the impedance of the signal line as taught by Nishiuma et al (abstract, first line), it would have been obvious to include the further limitation in claim 9 of the invention that the performance characteristics to be used as input into the selection of the impedance value of said wire would be defined at least in part by the impedance of the transistor.

With regard to claim 11: because it is common knowledge in the entire art of electromagnetism that the impedance of a wire of constant constitution and cross section depends linearly on its length, following from the elementary law that the impedance of any given circuit is the algebraic sum of the impedances of all components when all components are connected in series, it would have been obvious for purposes of impedance control to select the required wire impedance referred to in claim 9 by selecting the number of wires to make (at least) one electrical connection of the transistor circuit.

With regard to claim 12: continuing the discussion for claim 11 given just above: since it is the overall length of a wire upon which the impedance depends linearly, and because length is easily varied without the need to vary any of the other properties of a wire such as cross section and constitution, it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation in claim 9 that the required wire impedance is determined by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

With regard to claims 1 – 4: the power transistor circuit of claims 9 – 12 would necessarily have to be made in order to function. Claims 1 – 4 fail to further limit the power transistors of claims 9 – 12 other than simply require their formation.

3. *Claims 5 – 8 and 13 - 16 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Kagawa (5,371,405) in view of Nishiuma et al (JP404048756A). Kagawa teaches a high-power transistor (cf. title) comprising

a substrate 2 (cf. Fig. 1(a) and column 2, line 38);

a transistor chip or die 6 secured to the substrate (cf. column 2, line 67-68), the die comprising a transistor (die is called 'transistor chip') having an output terminal (cf. claims 1 and 12 in Kagawa) (the terminal connected to wire 23 or wire 25 (cf. column 3, line 19-28));

an output matching element in the form of a MOS capacitor 8 (cf. column 3, lines 29-34) (or any other capacitor; see column 2, lines 59-62) secured to the substrate by means of ground pad 3 (cf. column 2, line 41); and

one or more wires (wires 23 or 25) coupling the transistor die 5 (or 6: 5 and 6 point to the same component type in all figures) electrically coupling the transistor input terminal to the output matching element 8.

Kagawa does not necessarily teach the impedance of wire 23 or wire 25 to be based in part on a performance characteristic of the transistor measured after the die is secured to the substrate.

However, it is widely known in the art of high-frequency power transistors that particularly for high-frequency applications the impedance of the wires is important and needs to be tailored to other device components, as witnessed by Nishiuma et al, who teach to make the impedance of a bonding wire to coincide with the impedance of a signal line as part of the design of a semiconductor integrated circuit for high-frequency signal propagation (see 'abstract', first sentence, and 'constitution', final sentence). Furthermore, the bonding wires, being the final components to be added to the device as a whole, are the last components of which the impedance is still controllable, after the transistor die has been secured to the substrate. It thus would be obvious to measure the impedance characteristics of the die thus secured to the substrate prior to selecting the impedance of the wire for the purpose of impedance control of the IC. In summary, it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the stipulation in claim 13 that the impedance of the said one or more wires be selected or based at least in part on the performance characteristics of the transistor as measured after the die is secured to the substrate.

With regard to claim 14: because matching of one impedance to another impedance is an important parameter to control, as witnessed for instance by the matching of the impedance of said bonding wire to the impedance of the signal line as taught by Nishiuma et al (abstract, first line), it would have been obvious to include the further limitation in claim 13 of the invention that the performance characteristics to be

used as input into the selection of the impedance value of said wire would be defined at least in part by the impedance of the transistor.

With regard to claim 15: because it is common knowledge in the entire art of electromagnetism that the impedance of a wire of constant constitution and cross section depends linearly on its length, following from the elementary law that the impedance of any given circuit is the algebraic sum of the impedances of all components when all components are connected in series, it would have been obvious for purposes of impedance control to select the required wire impedance referred to in claim 13 by selecting the number of wires to make (at least) one electrical connection of the transistor circuit.

With regard to claim 16: continuing the discussion for claim 15 given just above: since it is the overall length of a wire upon which the impedance depends linearly, and because length is easily varied without the need to vary any of the other properties of a wire such as cross section and constitution, it would have been obvious to one of ordinary skills in the art to modify the invention at the time it was made so as to include the further limitation in claim 13 that the required wire impedance is determined by selecting a length of at least one wire used to make at least one electrical connection of the transistor circuit.

With regard to claims 5 – 8: the power transistor circuit of claims 13 – 16 would necessarily have to be made in order to function. Claims 5 – 8 fail to further limit the power transistors of claims 13 – 16 other than simply require their formation.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Goto et al. (6,281,756 B1) ;

W.R. Smythe, "Static and Dynamic Electricity", McGraw-Hill Book Company, New York, 1950 (Second Edition, page 360).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nathan Flynn
Supervisory Patent Examiner

JPM
January 10, 2002